

What Is Claimed Is:

1 1. A level-shifting circuit, comprising:
2 a level modulating circuit having an input terminal and an
3 inverse input terminal for respectively receiving a
4 complementary pair of small signals, and a first
5 output terminal for outputting a voltage level in
6 response to the complementary pair of small signals;
7 and
8 an enable circuit coupled to the first output terminal and
9 making the first output terminal output a
10 predetermined voltage level signal when receiving a
11 disable signal.

1 2. The level-shifting circuit as claimed in claim 1,
2 wherein the enable circuit is a MOS transistor having a source
3 and a drain coupled between an external level and the first
4 output terminal, and a gate coupled to the disable signal.

1 3. The level-shifting circuit as claimed in claim 2,
2 wherein the enable circuit is a first PMOS transistor having the
3 source coupled to a power source, and the drain coupled to the
4 first output terminal.

1 4. The level-shifting circuit as claimed in claim 2,
2 wherein the enable circuit is a first NMOS transistor having the
3 source coupled to a ground level, and the drain coupled to a
4 second output terminal.

1 5. The level-shifting circuit as claimed in claim 1,
2 wherein the enable circuit further comprises a pair of second
3 NMOS transistors having drains respectively coupled to the input
4 terminal and the inverse input terminal, sources coupled to the

5 complementary pair of small signals, and gates coupled to the
6 disable signal.

1 6. The level-shifting circuit as claimed in claim 4,
2 wherein the enable circuit further comprises a pair of third NMOS
3 transistors having drains respectively coupled to the input
4 terminal and the inverse input terminal, sources coupled to the
5 complementary pair of small signals, and gates coupled to the
6 disable signal.

1 7. The level-shifting circuit as claimed in claim 6,
2 wherein the enable circuit further comprises an inverter coupled
3 between the gates of the first and third NMOS transistors.

1 8. The level-shifting circuit as claimed in claim 1,
2 wherein the level modulating circuit comprises:

3 a first PMOS transistor having a first gate coupled to the
4 input terminal, a first source coupled to a power
5 source and a first drain as the second output
6 terminal;

7 a second PMOS transistor having a second gate coupled to
8 the reverse input terminal, a second source coupled
9 to and a second drain as the first output terminal;

10 a third NMOS transistor having a third gate coupled to the
11 power source, a third drain coupled to the first drain
12 and a third source as the input terminal; and

13 a fourth NMOS transistor having a fourth gate coupled to
14 the power source, a fourth drain coupled to the second
15 drain and a fourth source as the inverse input
16 terminal.

1 9. A level-shifting circuit, comprising:

2 a level modulating circuit having a first input terminal
3 for receiving a reference signal and a second input
4 terminal for receiving a modulating signal, and an
5 output terminal for outputting a voltage level in
6 response to the level of the modulating signal; and
7 an enable circuit coupled to the output terminal and making
8 the output terminal output a predetermined voltage
9 level signal when receiving a disable signal.

1 10. The level-shifting circuit as claimed in claim 9,
2 wherein the enable circuit is a thin film transistor (TFT) having
3 a source and a drain coupled between an external level and the
4 output terminal, and a gate coupled to the disable signal.

1 11. The level-shifting circuit as claimed in claim 9,
2 wherein the enable circuit is a first P-type thin film transistor
3 having the source coupled to a power source, and the drain
4 coupled to the first output terminal.

1 12. The level-shifting circuit as claimed in claim 9,
2 wherein the enable circuit is a first N-type thin film transistor
3 having the source coupled to a ground level, and the drain
4 coupled to a second output terminal.

1 13. The level-shifting circuit as claimed in claim 9,
2 wherein the enable circuit further comprises a pair of second
3 N-type thin film transistors having drains respectively coupled
4 to the first and second input terminals, sources respectively
5 receiving the reference signal and the modulating signal, and
6 gates coupled to the disable signal.

1 14. The level-shifting circuit as claimed in claim 9,
2 wherein the enable circuit further comprises a pair of third
3 N-type thin film transistors having drains respectively coupled

4 to the first and second input terminals, sources respectively
5 receiving the reference signal and the modulating signal, and
6 gates coupled to the disable signal.

1 15. The level-shifting circuit as claimed in claim 9,
2 wherein the enable circuit further comprises an inverter coupled
3 between the gates of the first N-type thin film transistor and
4 the third N-type thin film NMOS transistor.